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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,169	03/01/2004	Adrian C. Moga	BEA920030024US1	1020

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,169	MOGA ET AL.	
	Examiner	Art Unit	
	Zhuo H. Li	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/1/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement filed on March 1, 2004 has been considered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Cypher et al. (US Pub. 2004/0,002,992 hereinafter Cypher).

Regarding claim 1, Cypher discloses a cache coherent system (900, figure 9) comprising a memory, i.e., memory subsystem (144, figure 1), having a plurality of memory unit, a plurality of nodes (920, figure 9) employing a coherence protocol to maintain cache coherence of the memory (page 2 [0028] and page 8 [0078]), a cache (280, figure 2A) within each node to temporarily store contents of the plurality of memory units (page 2 [0029], and logic, i.e., switch (200, figure 2A) within each node (140, figure 1) to determine whether a cache miss relating to a memory nit should be transmitted to one or more nodes lesser in number than the plurality of nodes based on a criteria (pages 3-4, [0036] to [0039]).

Regarding claim 2, Cypher discloses the criteria includes whether to ultimately reach an owning node for the memory unit, such transmission is likely to reduce total communication traffic among the plurality of nodes and unlikely to increase latency as compared to broadcasting the cache miss to all the plurality of nodes, i.e., point-to-point mode transmissions (page 3, [0039], and pages 6-7 [0067] to [0074]).

Regarding claim 3, Cypher discloses the logic wherein each node is to determine whether the node is a home node for the memory unit to which the cache miss relates in determining that transmission to the one or more nodes lesser in number than the plurality of nodes is likely to reduce total communication traffic among the plurality of nodes and unlikely to increase latency to ultimately reach the owning node for the memory unit (page 3 [0038] to [0039]).

Regarding claim 4, Cypher discloses the one or more nodes comprise an owning node for the memory unit as stored at a directory (220, figure 2) of the home node (pages 4-5, [0048] to [0051]).

Regarding claim 5, Cypher discloses the logic, i.e., switch (200, figure 2A) within each node is to determine whether the cache of node has store a hint, i.e., mode table stores a plurality of memory units with its corresponding state, ownership, location and transfer mode information, along with the requested memory unit information stored in directory, as to a potential owning node for the memory unit as a result of an earlier event in determining that transmission to the one or more nodes lesser in number than the plurality of nodes is likely to reduce total communication traffic among the plurality of nodes and unlikely to increase latency to ultimately reach the owning node for the memory unit (pages 6-7, [0065] to [0070]).

Regarding claim 6, Cypher disclose the event includes an invalidation of the memory unit by the potential owning node, i.e., slave agent (104, figure 8A), and (pages 6-7, [0065] to [0070]).

Regarding claim 7, Cypher discloses the one ore more nodes comprises a home node of the memory unit and the potential owning node for the memory unit (page 6 [0065] to [0066]).

Regarding claim 8, Cypher discloses the logic within each node is to determine whether the memory unit relates to a predetermined memory sharing pattern encompassing the one or more nodes in determining that transmission to the one or more nodes lesser in number than the plurality of nodes s likely to reduce total communication traffic among the plurality of nodes and unlikely to increase latency to ultimately reach the owning node for the memory unit (pages 3-5, [0039], [0042], [0046] and [0054] to [0055]).

Regarding claim 9, Cypher discloses a method comprising steps of determining at a first node whether a cache miss relating to a memory unit of a shared memory system of a plurality of nodes including the first node and employing a coherence protocol should be selectively broadcast to one or more nodes lesser in number than the plurality of nodes based on a criteria (page 3 [0038]), in response to determining that the cache miss should be selectively broadcast, i.e., point-to-point transmission, to the one or more nodes, selectively broadcasting the cache miss by the first node to the one or more nodes (page 3 [0039]).

Regarding claim 10, Cypher discloses the method further comprising in response to determining that the cache miss should not be selectively broadcast, i.e., point-to-point transmission, to the one or more nodes, broadcasting the cache miss by the first node to all of the plurality of nodes, i.e., broadcast mode, (page 3 [0039]).

Regarding claim 11, the limitations of the claim are rejected as the same reasons set forth in claim 2.

Regarding claim 12, Cypher discloses the method further comprising step of determining whether the cache miss should be selectively broadcast, i.e., point-to-point transmission, to the one or more nodes comprises determining whether the first node is a home node for the memory unit, such that selectively broadcasting the cache miss to the one or more nodes comprises selectively broadcasting the cache miss to one node of the plurality of nodes as an owning node for the memory unit as stored at a directory (220, figure 2A) of the first node as the home node for the memory unit (page 3, [0038] to [0039], and page 5 [0048]).

Regarding claim 14, the limitations of the claim are rejected as the same reasons set forth in claim 8.

Regarding claim 15, the limitations of the claim are rejected as the same reasons set forth in claim 9.

Regarding claim 16, Cypher discloses a method comprising determining at a first node, i.e., requested agent, whether a cache miss relating a memory unit of a shared memory system (900, figure 9) of a plurality of nodes (920, figure 9) including the first node should be selectively broadcast, i.e., point-to-point transmit, to one or more other nodes of the plurality of nodes, based on whether the first node is a home node for the memory unit (page 3 [0037] to [0039]), or whether the first node has a pre-stored hint as to a potential owning node for the memory unit, i.e., mode table stores a plurality of memory units with its corresponding state, ownership, location and transfer mode information, along with the requested memory unit information stored in directory, in response to determining that the cache miss should be

selectively broadcast to the one or more other nodes, selectively broadcasting the cache miss by the first node to the one or more other nodes (figure 8A and 8B, and pages 6-7, [0065] to [0070]), otherwise, determining at the first node whether the memory unit relates to a predetermined memory sharing pattern encompassing a sub-plurality of the plurality of nodes smaller in number than the plurality nodes, i.e., encompassing a sub-plurality of nodes by grouping the related nodes together (pages 3-5, [0039], [0042], [0046] and [0054] to [0055]), and in response to determining that the memory unit relates to the predetermined memory sharing pattern, selectively broadcasting the cache miss by the first node to the sub-plurality of the plurality of nodes (figures 8A and 8B, and pages 6-7, [0065] to [0070] and [0074]).

Regarding claim 17, Cypher discloses a node (920, figure 9) of a system (900, figure 9) having a plurality of nodes (figure 9) comprising local memory (144, figure 2A) for which the node is a home node and that is shared among the plurality of nodes (page 2 [0030]), a directory (220, figure 2A) to track which of the plurality of nodes has cached or modified the local memory of the node (pages 4-5, [0048] to [0051]), a cache (280, figure 2A) to temporarily store contents of the local memory and memories of another ones of the plurality of nodes (page 2 [0029]), and logic, i.e., switch (200, figure 2A), to determine whether a cache miss relating to a local memory should be transmitted to one or more nodes lesser in number than the plurality of nodes based on whether, to ultimately reach an owning node for the local memory, such transmission is likely to reduce total communication traffic among the plurality of nodes and unlikely to increase latency as compared to broadcasting the cache miss to all of the plurality of nodes (page 3 [0036] to [0039]).

Regarding claim 18, Cypher discloses an article of manufacture comprising a computer-readable medium, and means in the medium for selectively broadcasting, i.e., point-to-point transmit, a cache miss relating to a memory unit of a shared memory system (900, figure 9) of a plurality of nodes (920, figure 9) employing a coherence protocol to one or more nodes lesser in number than all the plurality of nodes of the shared memory system, based on a criteria (page 3 [0036] to [0039]).

Regarding claim 19, Cypher discloses an article of manufacture wherein the means is for selectively broadcasting the cache miss to an owning node for the memory unit where an originating node the cache miss is a home node for the memory unit where an originating node of the cache miss is a home node for the memory unit (pages 6-7, [0067] to [0070]).

Regarding claim 20, Cypher discloses the article wherein the means is for selectively broadcasting, i.e., point-to-point transmit, the cache miss to a home node for the memory unit and a potential owning node, i.e., slave agent (104, figure 8B), for the memory unit where an originating node, i.e., request agent (100, figure 8B), of the cache miss has at a cache thereof a pre-stored hint, i.e., mode table stores a plurality of memory units with its corresponding state, ownership, location and transfer mode information, along with the requested memory unit information stored in directory, as to the potential owning node as a sending node of an earlier received invalidating of the memory unit (pages 6-7, [0065] to [0070]).

Regarding claim 21, Cypher discloses an article of manufacture wherein the means is for selectively broadcasting i.e., point-to-point transmit, the cache miss to a sub-plurality of the plurality of nodes smaller in number than the plurality of nodes where the memory unit relates to

a predetermined memory sharing pattern encompassing the sub-plurality of the plurality of nodes (pages 3-5, [0039], [0042], [0046] and [0054] to [0055]).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Glasco (US 2003/0,210,655) discloses method and apparatus for increasing the efficiency of data access in a multiple processor, multiple cluster system (abstract).

Singhal et al. (US PAT. 6,658,478) discloses a data storage system comprising a plurality of nodes for providing access to a data storage facility, and a plurality of communication paths interconnect the nodes, with a separate communication path provided for each two nodes of the data storage (col. 2 line 28 through col. 4 line 12).

Janakiraman et al. (US PAT. 6,704,842) discloses multiprocessor system with proactive speculative data transfer, wherein the system comprising a network memory, coherence controller in order to reduce latency in accessing data by performing proactive speculative data transfer (col. 3 line 55 through col. 4 line 27).

Van Doren et al. (US PAT. 6,209,065) discloses mechanism for optimizing generation of commit-signals in a distributed shared-memory system (abstract).

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 571-272-4183. The examiner can normally be reached on Tues - Fri 9:00am - 6:30pm and alternate Monday..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Zhuo H. Li

Patent Examiner
September 7, 2006

SANJIV SHAH
PRIMARY EXAMINER